**Lab 13**

**DDR SDRAM**



**Spring 2025**

Submitted by: **Mohsin Sajjad**

Registration No: **22pwsce2149**

Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (29 05, 2025)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

**DDR SDRAM**

**Objective:**

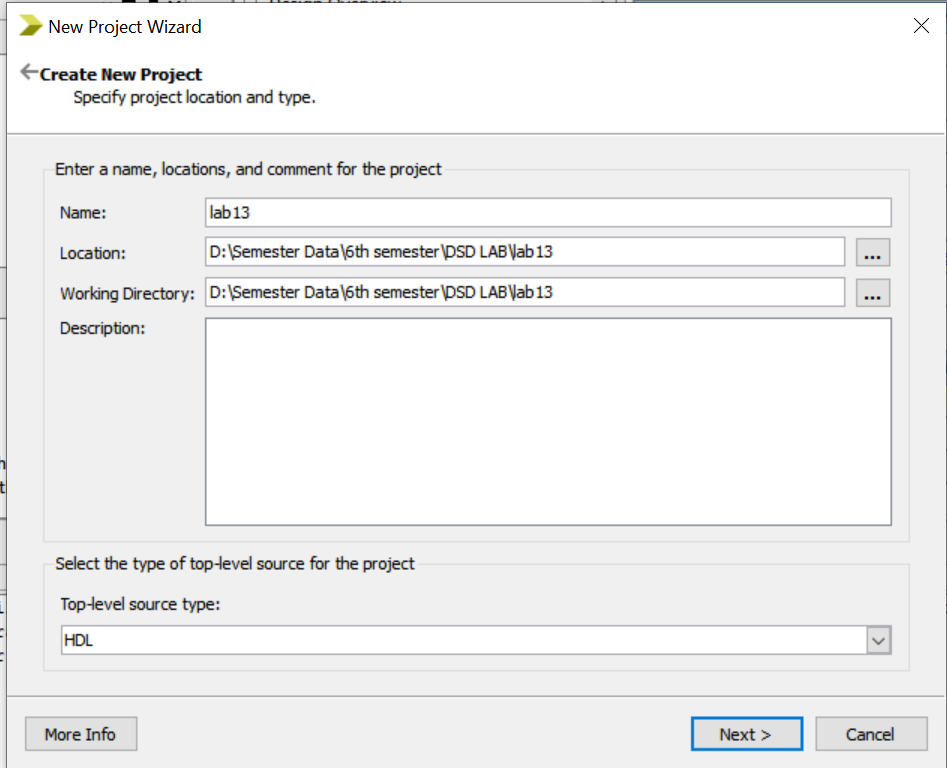
To interface and access DDR SDRAM (512Mbit LPDDR) on the Mimas V2 FPGA development board using Xilinx Spartan-6 and Xilinx ISE 14.7 tools.

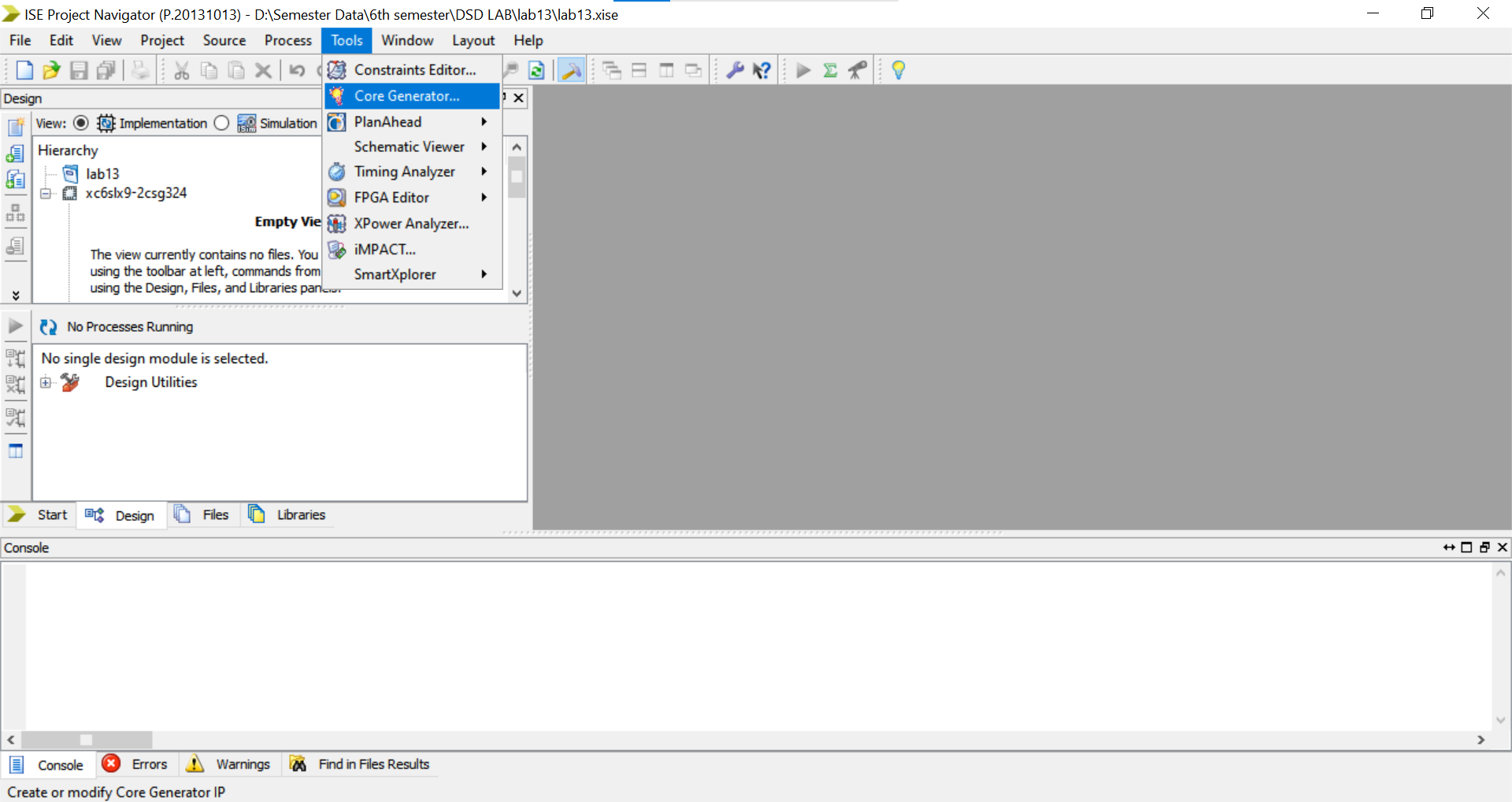
**DDR SDRAM**: High-speed, volatile memory used for storing data in FPGA-based applications.

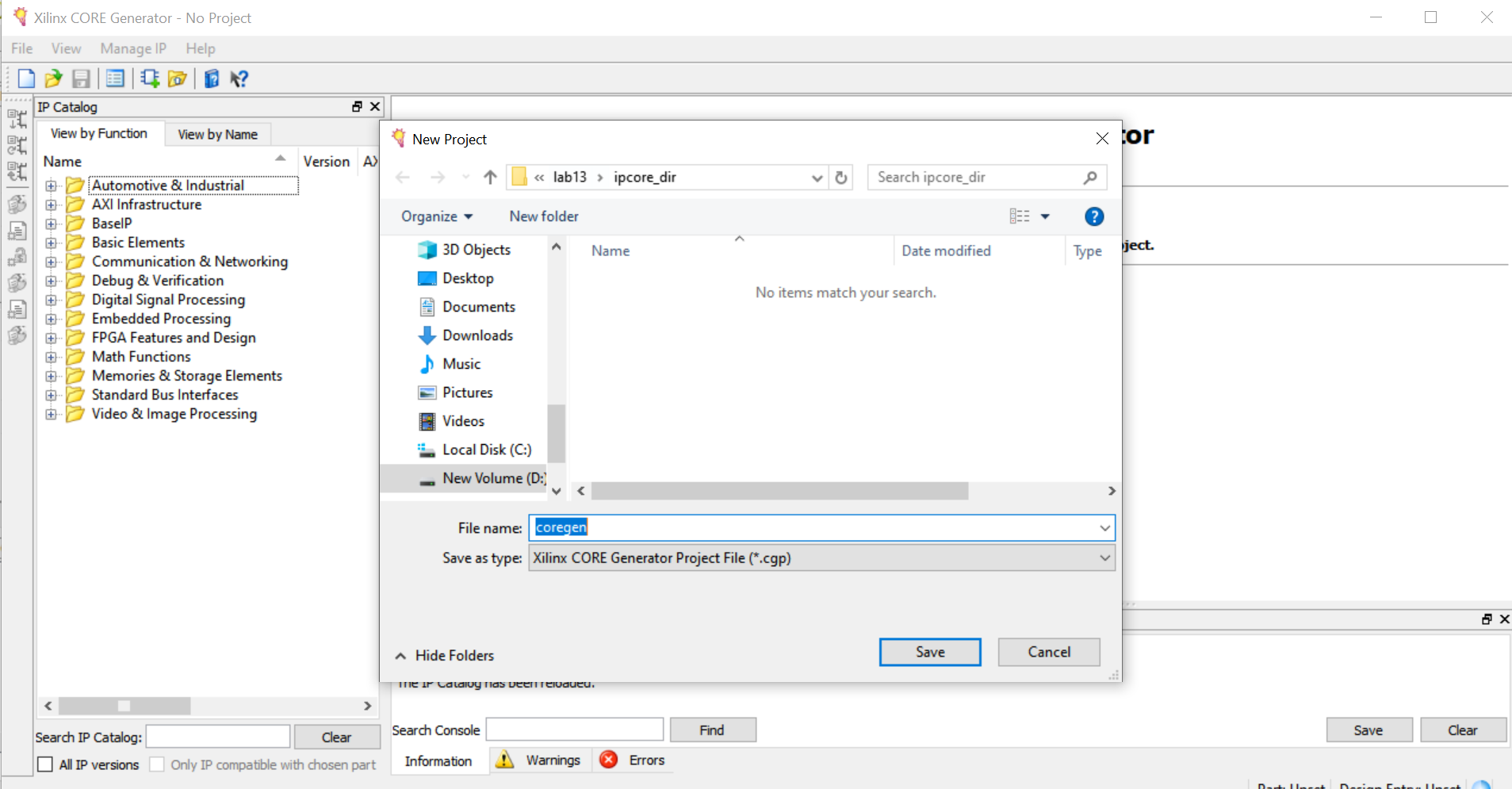
* **Memory Controller**: A logic block (hard or soft) that manages communication between FPGA and DDR.
* **Wrapper Logic**: Bridges user logic to memory controller with a simplified interface.
* **User Logic**: Your custom logic that reads/writes to memory.

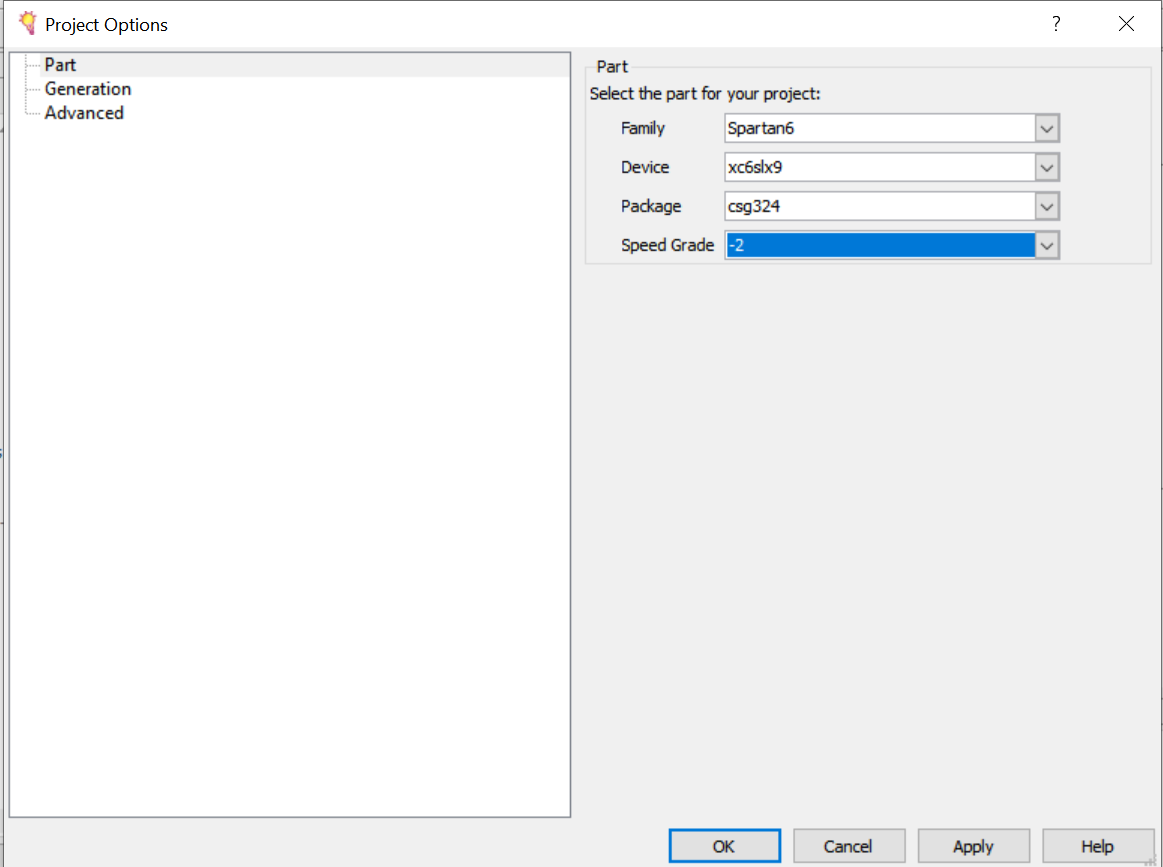
Spartan-6 LX9 (CSG324) includes **two built-in DDR memory controllers**; one is connected to onboard LPDDR on Mimas V2.

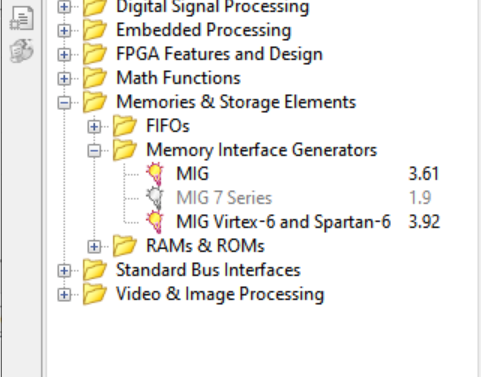
**STEPS:**

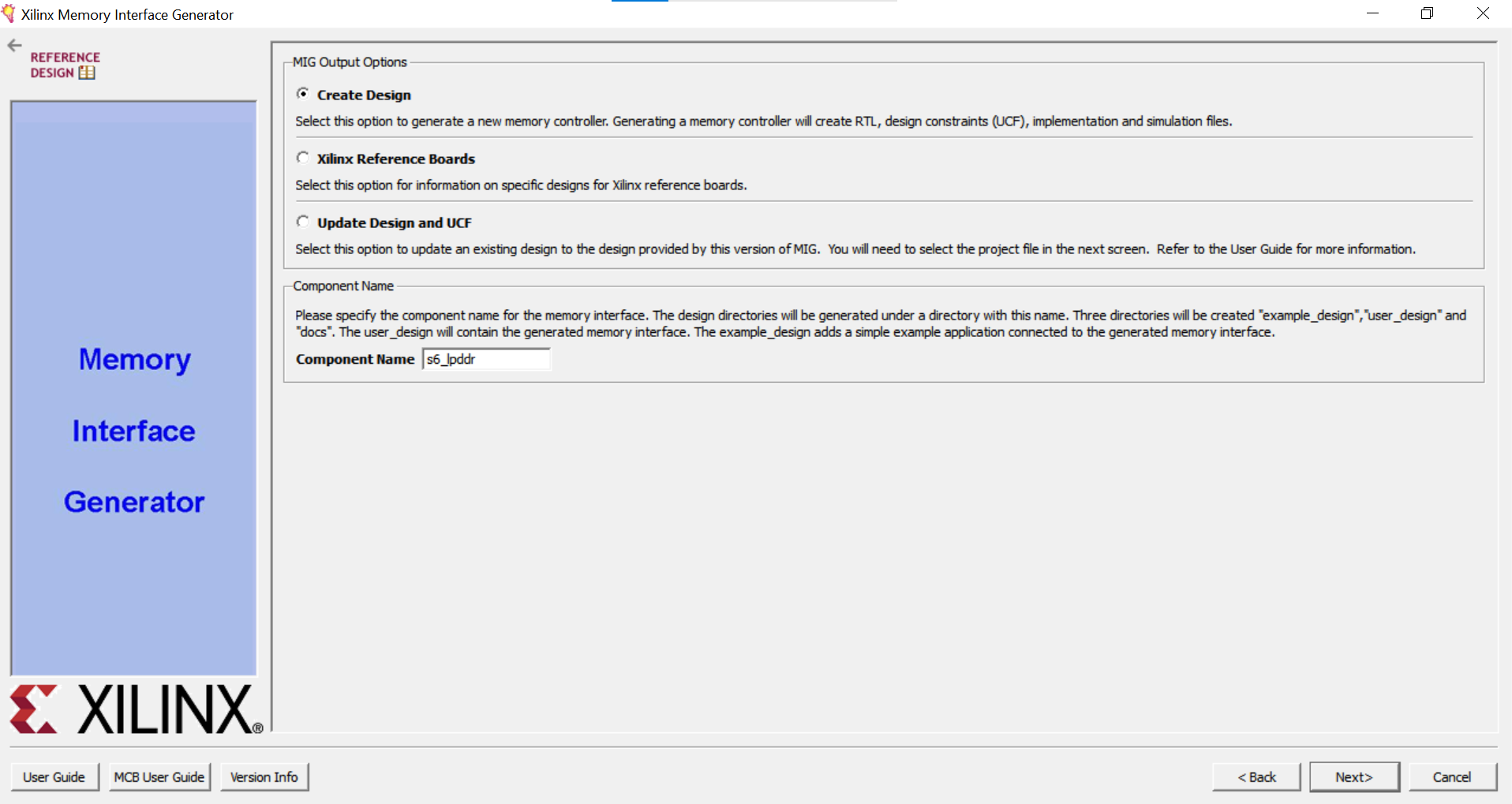
****

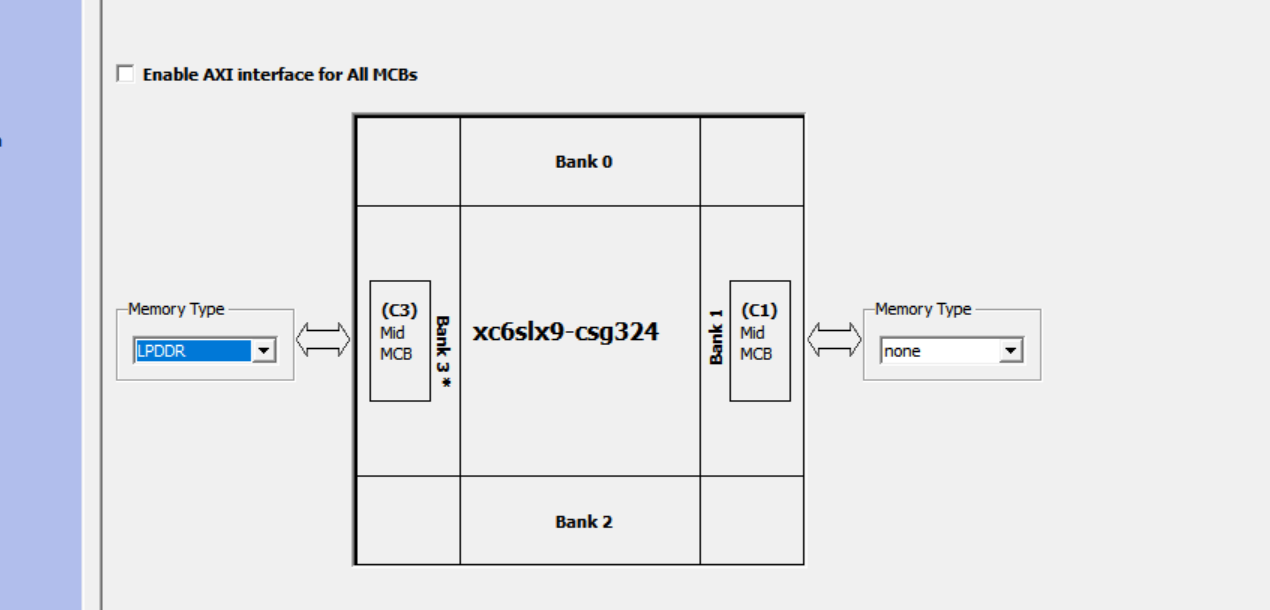
****

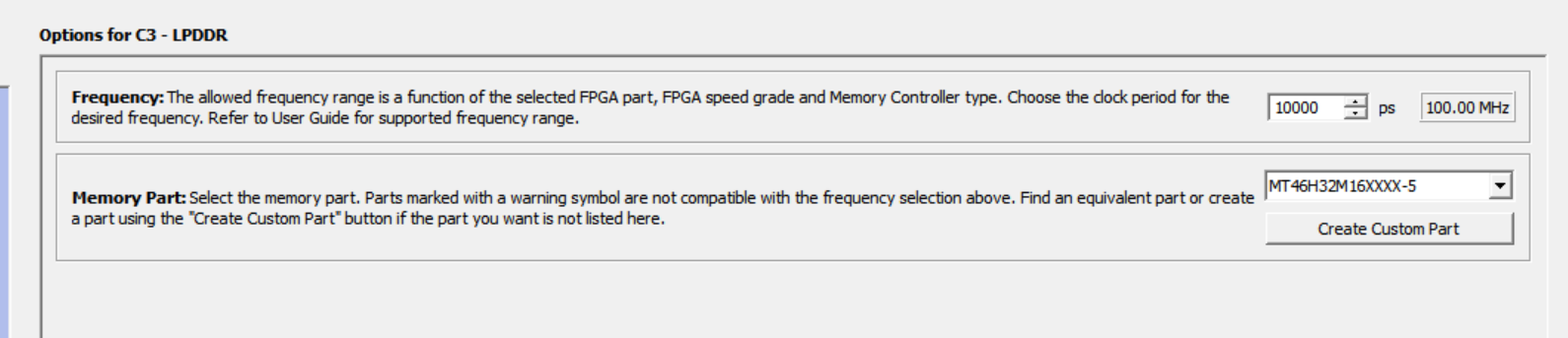
****

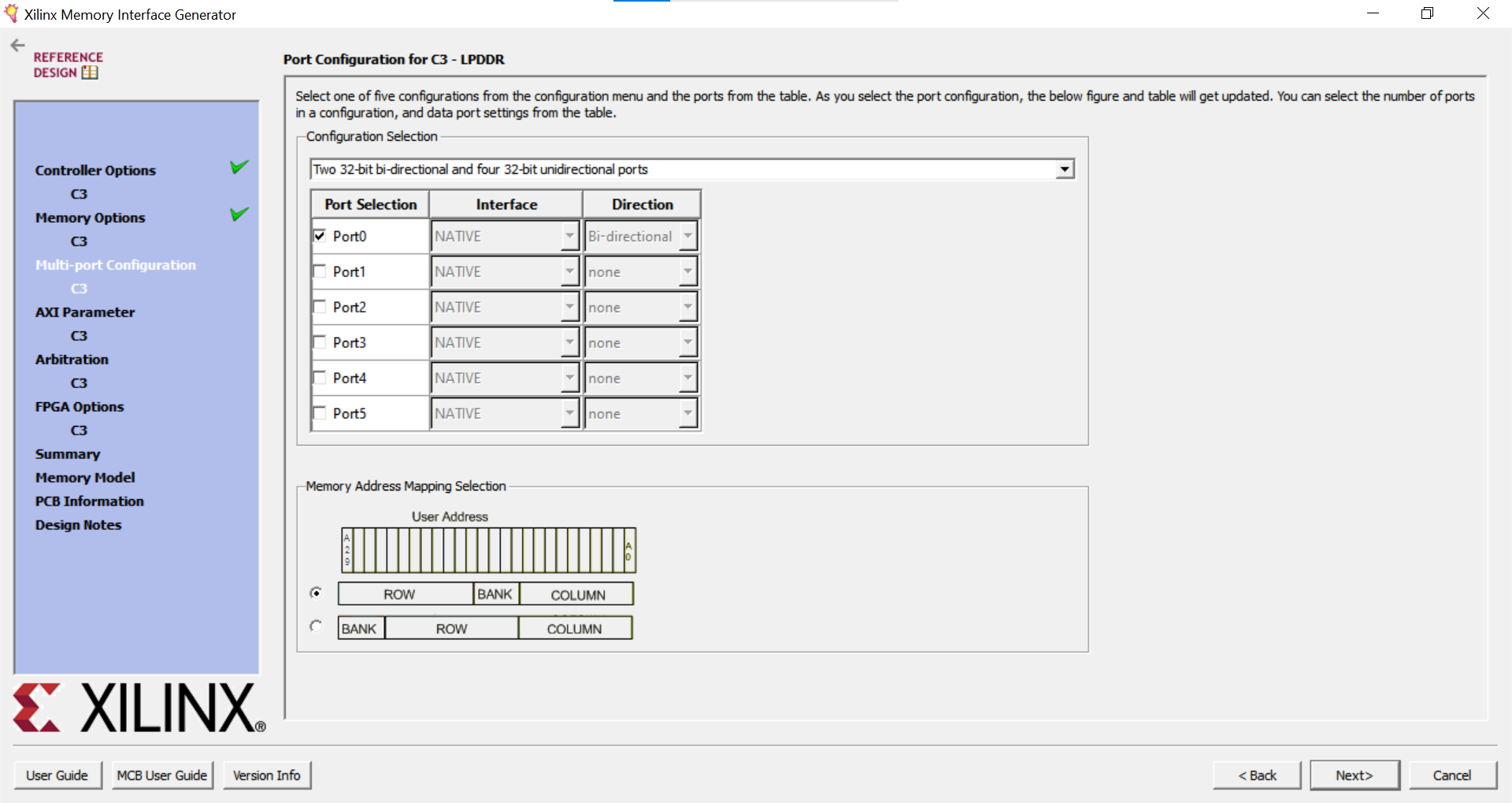
****

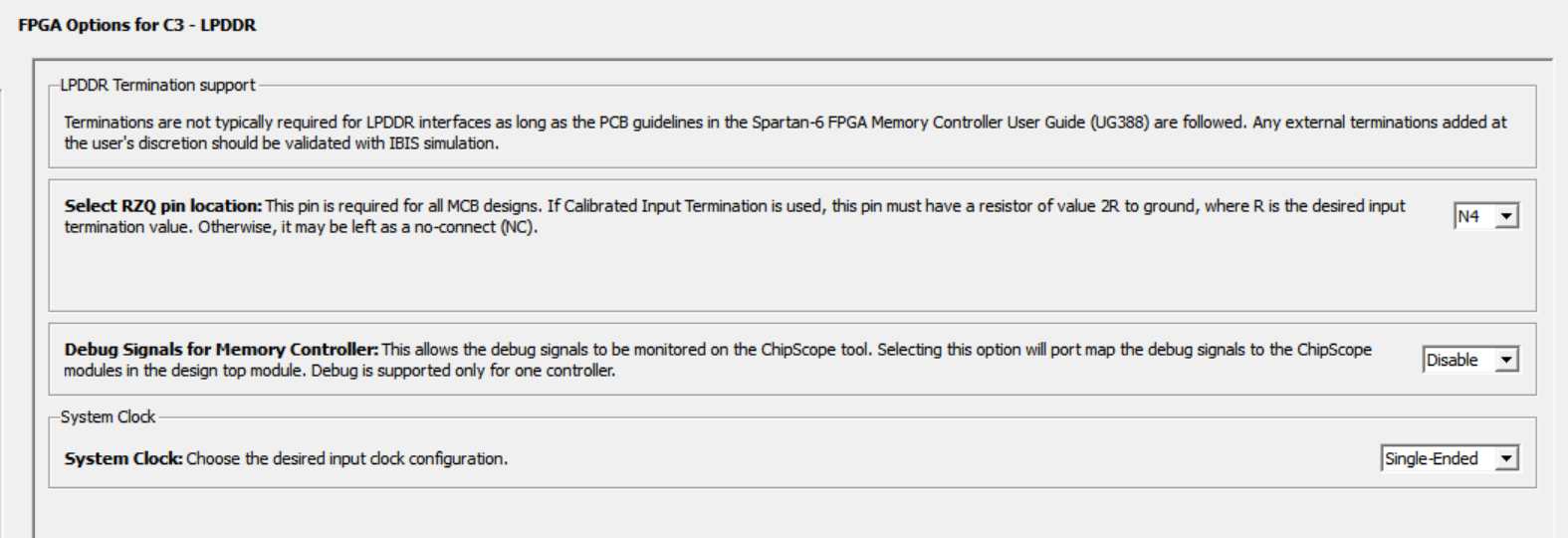
****

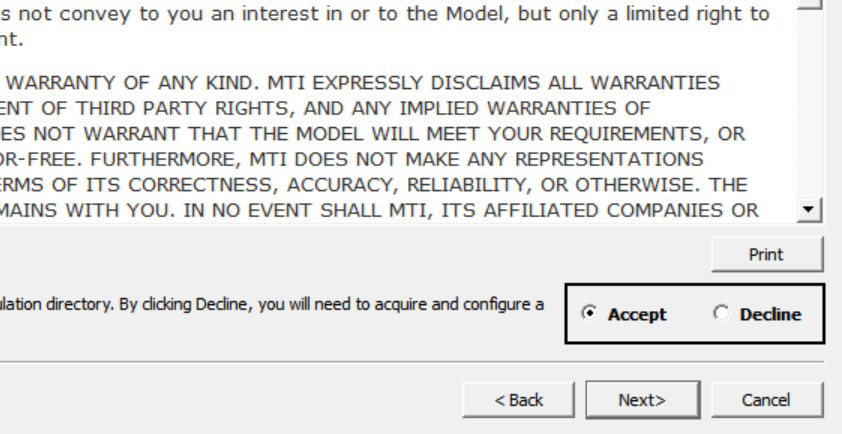
****

****

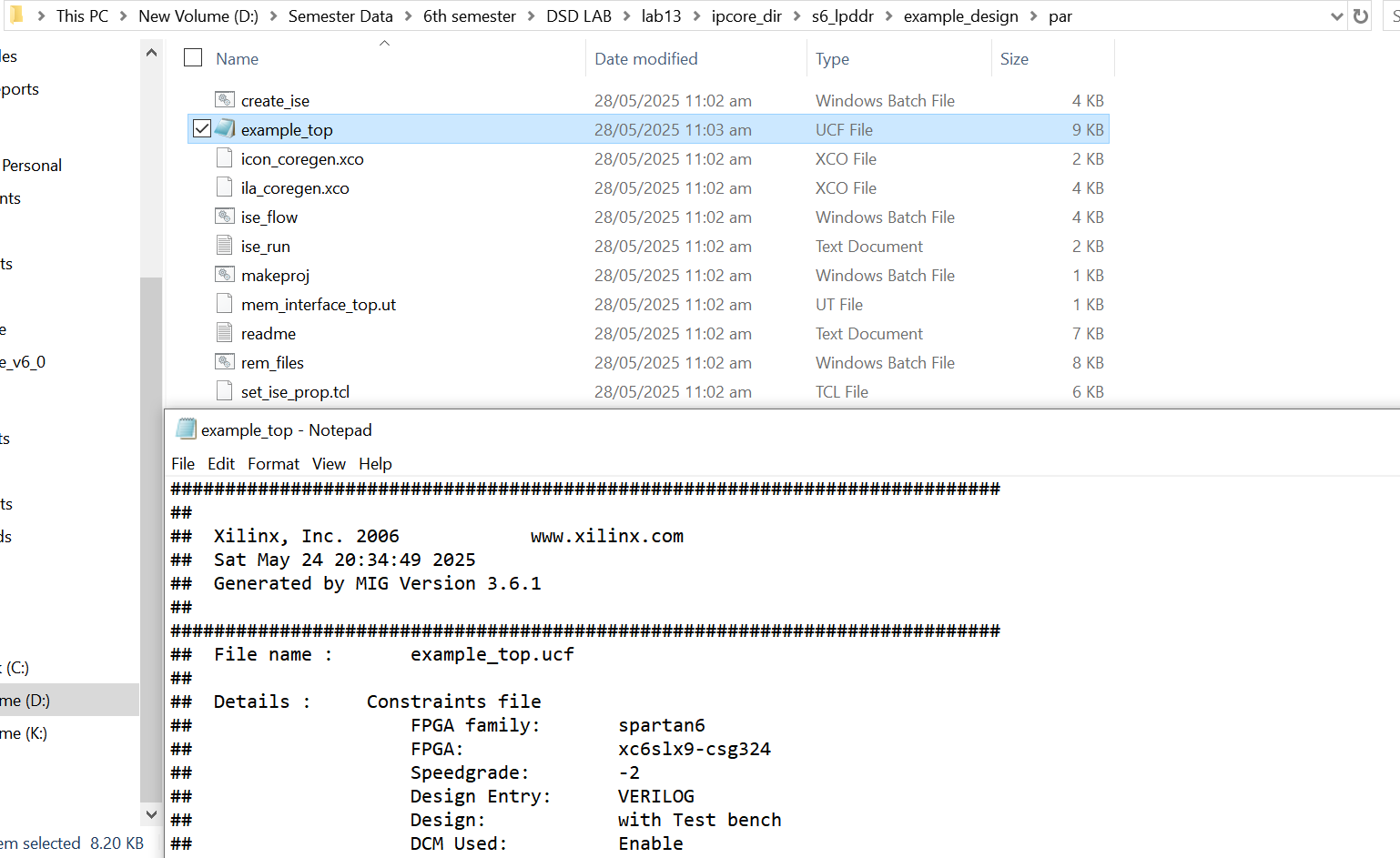
****

****

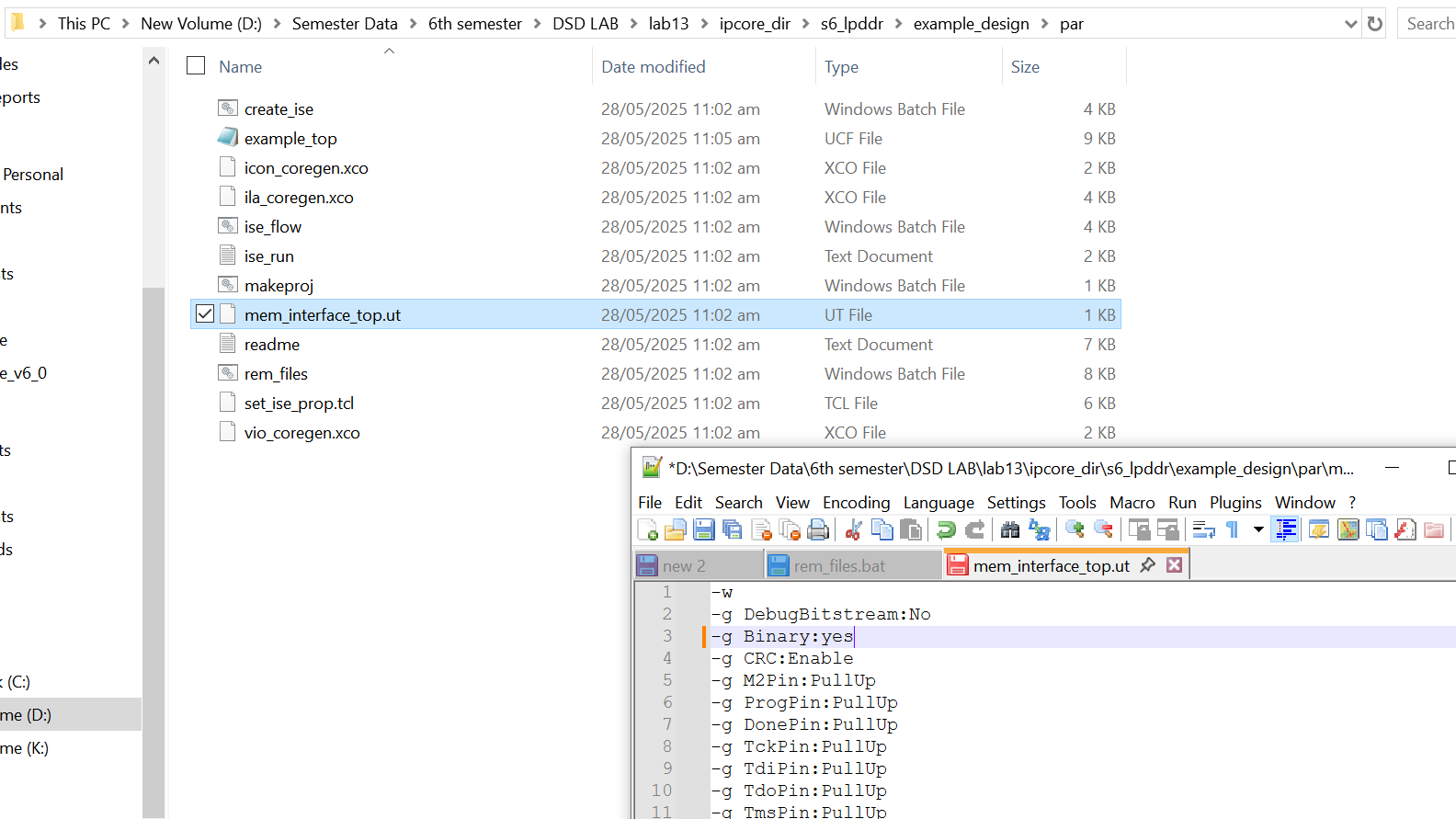
****

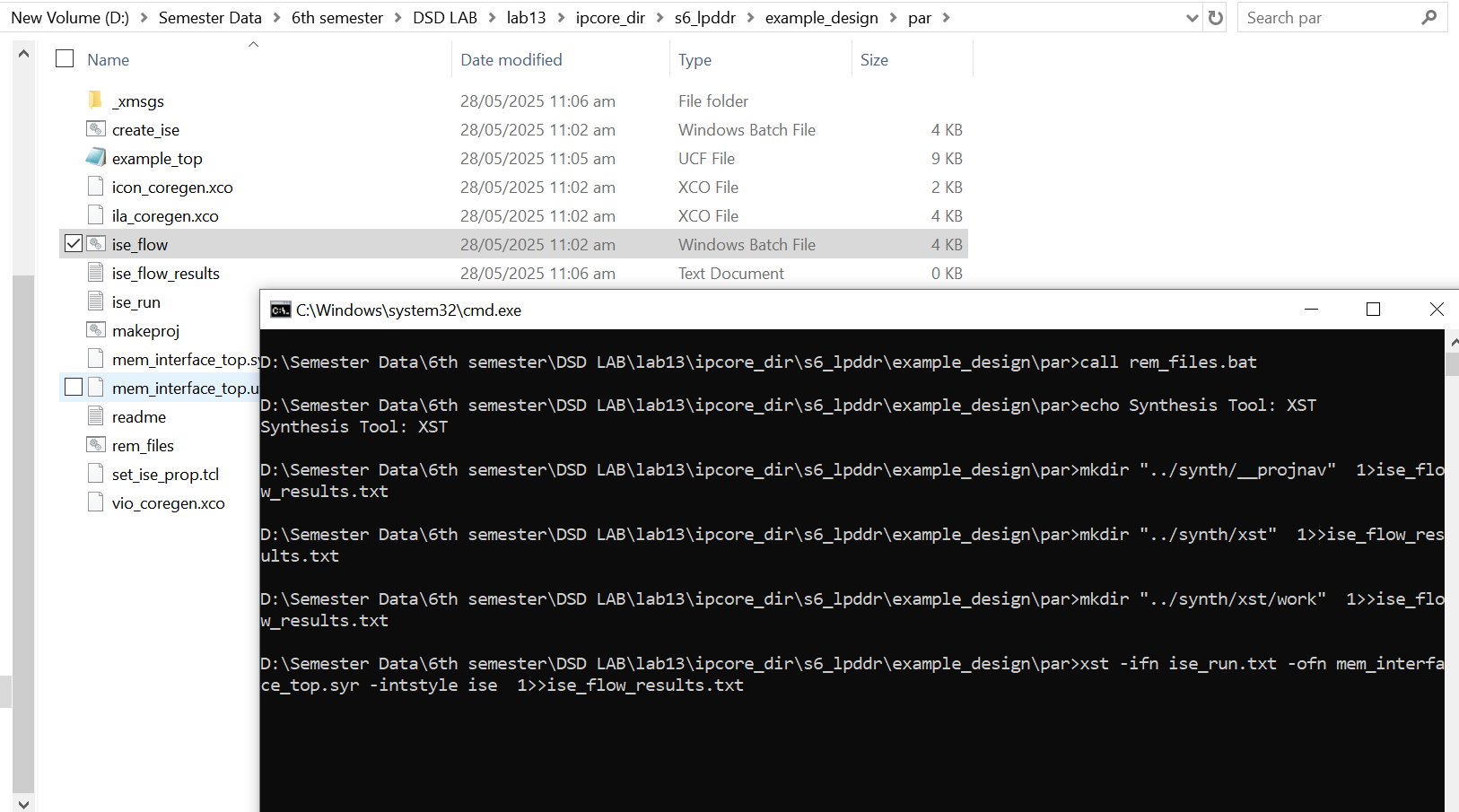
****

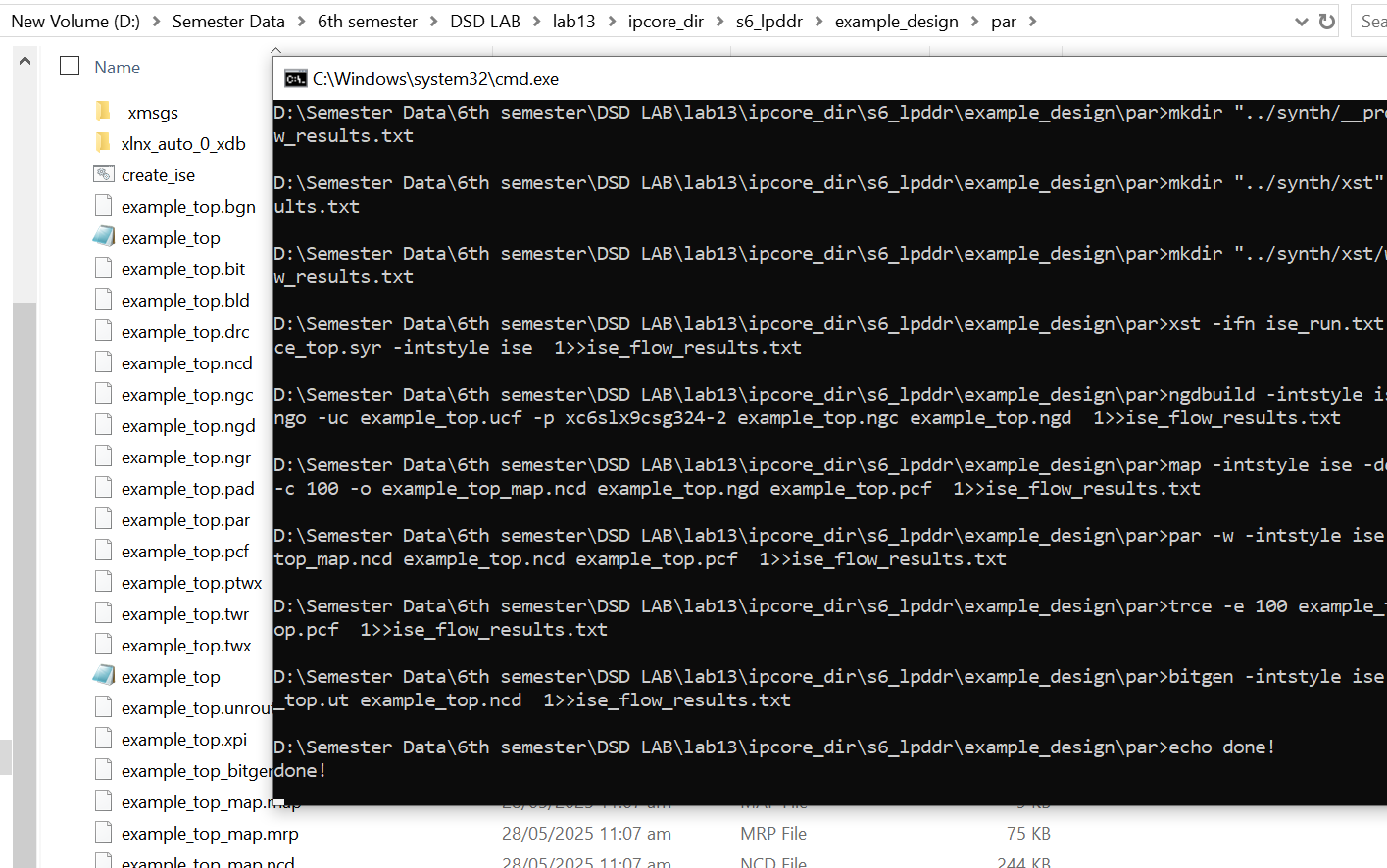
**Change example\_top**

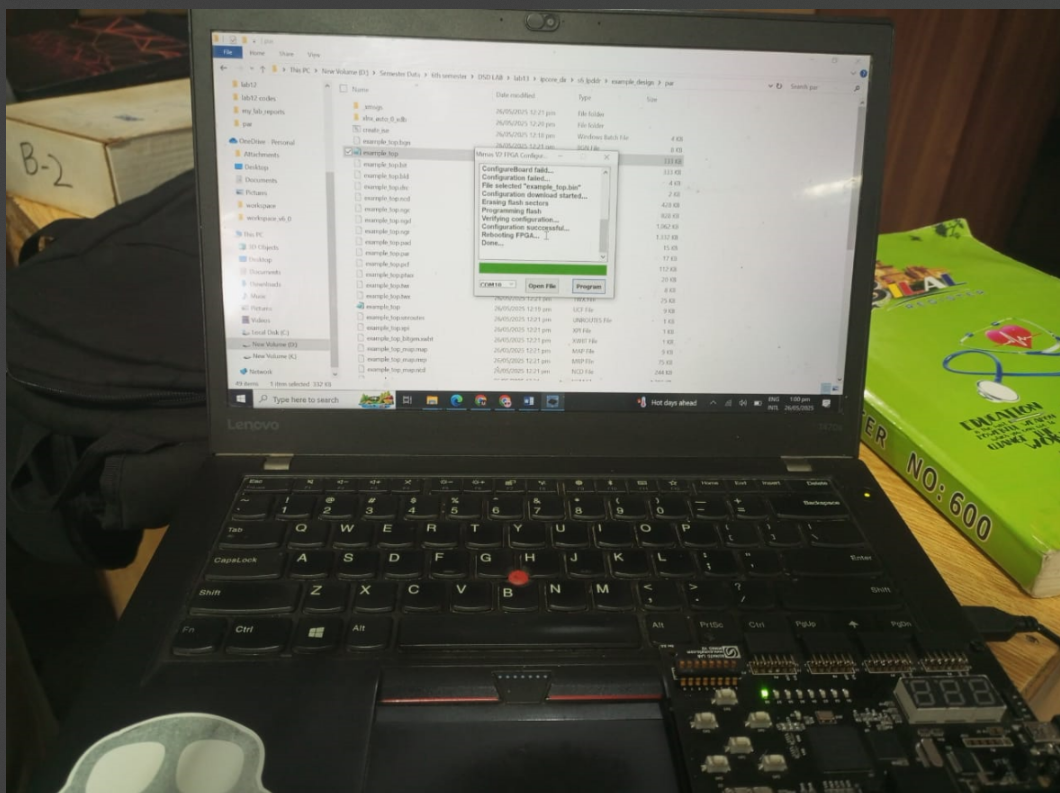
****

**Change mem\_interface\_top.ut**

****

**Run iso\_flow  
**

****

**Output:  
**